REMARKS

In response to the Office Action mailed April 21, 2004, Applicant has amended the application as above. No new matter is added by the amendments as discussed below. Applicant respectfully requests the entry of the amendments and reconsideration of the application in view of the amendments and the remarks set forth below.

Discussion of Claim Amendments

Claims 16-21 have been cancelled, without prejudice. Claims 1 and 4-15 have been amended. Claims 22-23 have been added. Upon the entry of the amendments, Claims 1-15 and 22-23 are pending in this application. The amendments to Claim 1 are supported by, for example, Figure 5. The amendments to Claims 4-15 are merely for clarification or to conform the claims to U.S. practice, and thus do not narrow the scope of protection. New Claim 22 is supported by, for example, the specification at page 5, lines 10-11. New Claim 23 is supported by, for example, the specification at page 6, lines 10-11. Thus, no new matter is added by the amendments. Applicant respectfully requests the entry of the amendments.

Discussion of Specification Objection

The Examiner objected to the specification asserting that the title of the invention is not descriptive. The Examiner notes that a new title is required that is clearly indicative of the invention to which the claims are directed. In reply, Applicant has amended the title from "Organic Thin Film Transistor (OTFT) and Manufacturing Process thereof" to "Organic Thin Film Transistor (OTFT)." Since all pending Claims are directed to an organic thin film transistor (OTFT), Applicant respectfully submits that the new title is clearly indicative of the invention to which the claims are directed. Withdrawal of the objection is respectfully requested.

Discussion of Claim Objections

The Examiner has objected to Claims 4-10 and 12-15 because the term "the said" is used in those claims. In reply, Applicant has amended the term to "the" in all of the objected claims. Withdrawal of the objections is respectfully requested.

Discussion of Claim Rejections Under 35 U.S.C. § 112, ¶ 2

The Examiner has rejected Claims 4 and 6-15 under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner asserts that in Claim 4, the term "said first insulation layer (3) is made of organic, inorganic or ferroelectric material" is unclear as to whether it is being referred to the first insulation layer (3) is selected from a group consisting of organic, inorganic or ferroelectric material. In reply, Applicant has amended the term to "the first insulation layer (3) is selected from a group consisting of organic, inorganic and ferroelectric material." Withdrawal of the claim rejection is respectfully requested.

The Examiner also notes that in Claims 11 and 14, the term "the said organic semiconductor layer" lacks antecedent basis. In reply, Applicant has amended the term "an active layer (7)" in Claim 1 to "an organic semiconductor layer (7)." Withdrawal of the claim rejections is respectfully requested.

Discussion of Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-15 under 35 U.S.C. § 103 (a) as being unpatentable over Yamazaki, et al. (U.S. Patent Application Publication No. 2002/0014624) in view of Klauk, et al. (A reduced complexity process for organic thin film transistors). Applicant respectfully traverses the Examiner's rejections as discussed below.

Standard of *Prima facie* Obviousness

In order to provide a *prima facie* showing of obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *See, e.g., In re Royka,* 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP 2143.03.

Patentability of Independent Claim 1

Claim 1 recites, among other things, i) the gate insulation layer including a first insulation layer (3) and a second insulation layer (4), wherein the first insulation layer and the substrate make contact, and ii) an organic semiconductor layer (7) which overlays the source and drain electrodes (5, 6), wherein the region comprising the source electrode and the drain electrode is separated from the first insulating layer by the second insulation layer. However, the above-

recited claim terms are neither taught nor suggested by the prior art references, alone or in combination.

1. **The Claim Terms "the gate insulation layer including a first insulation layer (3) and a second insulation layer (4)" and "wherein the first insulation layer and the substrate make contact" are neither Taught nor Suggested by Yamazaki and Klauk, Alone, or in Combination**

A) Discussion of Yamazaki

Referring to Figures 3A and 4A, Yamazaki clearly shows that the first insulation layer (303) and the substrate (300) do not make contact. Instead, the base film (silicon oxide; 301) makes contact with the first insulation layer (303). In addition, nowhere is there disclosure or teaching that wiring lines (302a-302c) can be directly formed on the substrate (300). Yamazaki further states that;

> First, a glass substrate is prepared as a substrate 300. A silicon oxide film with a thickness of 200 nm is formed thereon by sputtering as a base film 301. On the base film, first wiring lines 302a, 302b, and 302c are formed. The material of the first wiring lines is a tantalum film formed by sputtering. An oxide film may be formed on a surface of the tantalum film. *See the paragraph [0077] of Yamazaki*

That is, Applicant respectfully submits that in Yamazaki the silicon oxide base film (301) is required to be deposited between the substrate (300) and the first wiring lines (302a-302c) for proper wiring. Thus, the claim term "the first insulation layer and the substrate make contact" is neither taught nor suggested by Yamazaki.

B) Discussion of Klauk

Klauk neither teaches nor suggests the above-indicated claim term. Referring to Figure 1(a), Klauk clearly shows that there is only one insulation layer (gate dielectric layer). Furthermore, Klauk states that:

> The device structure shown in Fig. 1(a) requires four material depositions and four photolithography steps: One each for the gate electrode, the gate dielectric layer, the source/drain contacts, and the pentacene active layer. *See the third paragraph, left column, first page.*

Thus, the film transistor of Klauk requires four layers one of which is the gate dielectric layer. If the gate dielectric layer is modified to include two insulation layers, the Klauk transistor would be inoperable for its intended purpose because it would include more than four material depositions. MPEP 2143.01. Thus, the claim term "the gate insulating layer includes a first insulation layer and a second insulation layer" is neither taught nor suggested by Klauk.

C) Combination Neither Teaches Nor Suggests the Claim Terms

Since neither Yamazaki nor Klauk teaches or suggests "the gate insulation layer including a first insulation layer (3) and a second insulation layer (4), wherein the first insulation layer and the substrate make contact," the combination of the two references does not teach the above-indicated claim terms.

2. The Claim Terms "an organic semiconductor layer (7) which overlays the source electrode (5) and the drain electrode (6)" and "wherein the region comprising the source electrode and the drain electrode is separated from the first insulating layer by the second insulation layer" are neither Taught nor Suggested by Yamazaki and Klauk, Alone, or in Combination

A) Discussion of Yamazaki

Yamazaki does not teach or suggest that an organic semiconductor layer (7) overlays the source and drain electrodes (5, 6). Referring to Figures 3A and 3D (*see also Figures 4-5, 8-12, 16-17 and 21*), Yamazaki shows that an active layer (305, 306) is formed between the silicon oxide film (92) and the source and drain electrodes (326, 328). That is, Yamazaki discloses an active layer (305, 306) which underlays the source and drain electrodes (326, 328). In contrast, in the claimed invention, an organic semiconductor layer (active layer; 7) *overlays* the source and drain electrodes (5, 6).

Furthermore, Yamazaki does not teach or suggest that the region comprising the source electrode and the drain electrode is separated from the first insulating layer *by the second insulation layer*." It is clear from Figures 3A and 3D of Yamazaki that the source and drain electrodes (326, 328) are separated from the first insulating layer (303) by all of i) the active layer (305, 306), ii) the silicon oxide film (92) and iii) the second insulation layer (304). Yamazaki further states that:

> Next, a silicon oxide film 92 with a thickness of 10 nm is formed and an amorphous silicon film (not shown in the drawing) with a thickness of 50 nm is formed thereon successively without being exposed to the air. The applicant of the present invention has found that boron landed from the air on the bottom surface of an active layer affects TFT characteristics (especially the threshold voltage). However, this problem can be solved by forming a thin silicon oxide film and an amorphous silicon film in succession as in this embodiment. This silicon oxide film also functions as a barrier layer for preventing the tantalum oxide film to serve as the dielectric of the storage capacitor in the pixel matrix circuit from reacting with the active layer. *See the paragraph [0083] of Yamazaki*

It can be seen from the above that the silicon oxide film (92) and the active layer (305, 306) are necessary layers to perform the intended purpose of the Yamazaki process. Thus, if silicon oxide film (92) and the active layer (305, 306) are removed from the semiconductor structure such that there exists only the second insulation layer (304) between the first insulation layer (303) and the source/drain electrodes (326, 328), the Yamazaki process would be inoperable for its intended purpose. MPEP 2143.01. Thus, Applicant respectfully submits that the claim term "the region comprising the source electrode and the drain electrode is separated from the first insulating layer *by the second insulation layer*" is neither taught nor suggested by Yamazaki.

B) Discussion of Klauk

Klauk does not teach or suggest the term "the region comprising the source electrode and the drain electrode is separated from the first insulating layer *by the second insulation layer*." As discussed above, since Klauk discloses only one insulation layer, the prior art reference cannot

show that the source electrode and the drain electrode are separated from the first insulating layer by the second insulation layer. *See Figure 1(a) of Klauk.*

C) Combination Does Not Teach or Suggest the Claim Terms

Since neither Yamazaki nor Klauk teaches or suggests "an organic semiconductor layer (7) which overlays the source and drain electrodes (5, 6), wherein the region comprising the source electrode and the drain electrode is separated from the first insulating layer by the second insulation layer," the combination of the two references does not teach the above-indicated claim terms.

3. There is No Motivation to Combine Yamazaki and Klauk to Arrive at the Claimed Invention

If proposed modification would render the prior art being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *MPEP 2143.01.*

As discussed above, Klauk requires four material depositions in the following order: i) the gate electrode, ii) the gate dielectric layer, iii) the source/drain contacts and the iv) active layer. *See Figure 1(a) of Klauk.* Referring to Figures 3A and 3D and as discussed above, Yamazaki requires at least i) base film layer (301), ii) the gate (302a), iii) the first insulation layer (303), iv) the second insulation layer (304), v) the silicon oxide film (92), vi) the active layer (305, 306) and vii) source/drain electrodes (326, 328) to perform its intended purpose. Thus, the modification of either Klauk or Yamazaki to arrive at the claimed structure (gate-first insulation-second insulation-source/drain-semiconductor (active) layer), which requires that at least one of the necessary layers of each prior art be removed, would render either Yamazaki or Klauk inoperable for its intended purpose.

4. Summary

In view of the above, the prior art references, alone or in combination, neither teach nor suggest i) the gate insulation layer including a first insulation layer (3) and a second insulation layer (4), wherein the first insulation layer and the substrate make contact, and ii) an organic

semiconductor layer (7) which overlays the source and drain electrodes (5, 6), wherein the region comprising the source electrode and the drain electrode is separated from the first insulating layer by the second insulation layer, recited in Claim 1. Thus, Applicant respectfully submits that no *prima facie* of obviousness has been established. Therefore, Claim 1 is allowable over the prior art of record.

Patentability of Dependent Claims

Claims 2-15 depend from base Claim 1, and further define additional technical features of the present invention. In view of the patentability of their base claim, and in further view of their additional technical features, dependent Claims 2-15 are patentable over the prior art of record.

Patentability of New Claims 22-23

Claims 22-23 depend from base Claim 1, and further define additional technical features of the present invention. In view of the patentability of their base claim, and in further view of their additional technical features, new Claims 22-23 are patentable over the prior art of record.

CONCLUSION

In view of Applicant's amendments to the application and the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. Should the Examiner have any remaining concerns which might prevent the prompt allowance of the application, the Examiner is respectfully invited to contact the undersigned at the telephone number appearing below.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 7/20/04

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